WE CLAIM:

1. A structure comprising:

an n-channel surface-channel insulated-gate field-effect transistor ("SCIGFET") comprising a pair of laterally separated n-type source/drain zones situated in a semiconductor body along a major surface thereof, a p-type channel zone situated between the n-channel SCIGFET's source/drain zones in the semiconductor body along its major surface, a gate electrode situated over the channel zone of the n-channel SCIGFET and extending partially over its source/drain zones, and a gate dielectric layer separating the gate electrode of the n-channel SCIGFET from its source/drain and channel zones; and

a normally off n-channel channel-junction insulated-gate field-effect transistor ("CJIGFET") comprising a pair of laterally separated n-type source/drain zones situated in the semiconductor body along its major surface, an n-type channel zone extending between the n-channel CJIGFET's source/drain zones in the semiconductor body along its major surface and more lightly doped than the n-channel CJIGFET's source/drain zones, a gate electrode situated over the channel zone of the n-channel CJIGFET and extending partially over its source/drain zones, and a gate dielectric layer separating the gate electrode of the n-channel CJIGFET from its source/drain and channel zones.

2. A structure as in Claim 1 wherein:

the gate electrode of the n-channel SCIGFET comprises n-type semiconductor material; and

the gate electrode of the n-channel CJIGFET comprises p-type semiconductor material.

3. A structure as in Claim 1 wherein the gate dielectric layer of the n-channel CJIGFET is thicker than the gate dielectric layer of the n-channel SCIGFET.

4. A structure as in Claim 1 wherein the n-channel CJIGFET is of greater channel length than the n-channel SCIGFET.

5. A structure as in Claim 1 wherein the n-channel CJIGFET conducts current through a field-induced channel.

6. A structure as in Claim 1 wherein the n-channel CJIGFET conducts current through a metallurgical channel.

7. A structure as in Claim 1 wherein the channel and source/drain zones of the n-channel CJIGFET contain arsenic as n-type dopant.

8. A structure as in Claim 1 further including a p-channel SCIGFET comprising a pair of laterally separated p-type source/drain zones situated in the semiconductor body along its major surface, an n-type channel zone extending between the p-channel SCIGFET's source/drain zones in the semiconductor body along its major surface, a gate electrode situated over the channel zone of the p-channel SCIGFET and extending partially over its source/drain zones, and a gate dielectric layer separating the gate electrode of the p-channel SCIGFET from its source/drain and channel zones.

9. A structure as in Claim 8 wherein:

the gate electrode of the n-channel SCIGFET comprises n-type semiconductor material; and

the gate electrodes of the p-channel SCIGFET and the n-channel CJIGFET comprise p-type semiconductor material.

10. A structure as in Claim 9 wherein the semiconductor material of the gate electrodes comprises non-monocrystalline semiconductor material.

11. A structure as in Claim 10 wherein the non-monocrystalline semiconductor material comprises polycrystalline semiconductor material.

12. A structure as in Claim 8 wherein the gate dielectric layer of the n-channel CJIGFET is thicker than the gate dielectric layers of the two SCIGFETs.

13. A structure as in Claim 12 wherein the gate dielectric layers of the two SCIGFETs are of approximately equal thickness.

14. A structure as in Claim 12 wherein the n-channel CJIGFET is of greater channel length than each SCIGFET.

15. A structure as in Claim 12 wherein:

the gate electrode of the n-channel SCIGFET comprises n-type semiconductor material; and

the gate electrodes of the p-channel SCIGFET and the n-channel CJIGFET comprise p-type semiconductor material.

16. A structure as in Claim 8 wherein the n-channel CJIGFET conducts current through a field-induced channel.

17. A structure as in Claim 16 wherein the gate dielectric layer of the n-channel CJIGFET is thicker than the gate dielectric layers of the two SCIGFETs.

18. A structure as in Claim 8 wherein the n-channel CJIGFET conducts current through a metallurgical channel.

19. A structure as in Claim 18 wherein the gate dielectric layer of the n-channel CJIGFET is thicker than the gate dielectric layers of the two SCIGFETs.

20. A structure as in Claim 8 wherein the channel and source/drain zones of the n-channel CJIGFET contain arsenic as n-type dopant.

21. A structure as in Claim 8 wherein the channel zone of each SCIGFET is part of body material having a net dopant concentration which reaches a primary local subsurface maximum below a channel surface depletion region that extends along the semiconductor body's major surface into that channel zone but no more than 0.4 μm below the semiconductor body's major surface.

22. A structure as in Claim 21 wherein the net dopant concentration of the body material for each SCIGFET reaches a pair of additional vertically separated local subsurface maxima deeper below the semiconductor body's major surface than the primary local subsurface maximum in the net dopant concentration for that body material.

23. A structure as in Claim 8 wherein the source/drain and channel zones of the n-channel CJIGFET form a composite pn junction with body material having a net dopant concentration which reaches a primary local subsurface maximum below the channel zone but no more than 0.6 μm below the semiconductor body's major surface.

24. A structure as in Claim 23 wherein the net dopant concentration of the body material for the n-channel CJIGFET reaches a pair of additional vertically separated subsurface maxima

deeper below the semiconductor body's major surface than the primary local subsurface maximum in the net dopant concentration for that body material.

25. A structure as in Claim 8 wherein the channel zone of each SCIGFET has a net dopant concentration which reaches a local subsurface minimum along the semiconductor body's major surface at a location between that SCIGFET's source/drain zones.

26. A structure as in Claim 25 wherein the channel zone of each SCIGFET is part of body material having a net dopant concentration which reaches a primary local subsurface maximum below a channel surface depletion region that extends along the semiconductor body's major surface into that channel zone but no more than 0.4 μm below the semiconductor body's major surface.

27. A structure as in Claim 8 wherein the three gate dielectric layers comprise semiconductor material and oxygen.

28. A structure as in Claim 27 wherein the gate dielectric layers of the two SCIGFETs further include nitrogen.

29. A structure as in Claim 27 wherein the semiconductor body and the semiconductor material in the three gate dielectric layers both comprise silicon.

30. A structure as in Claim 8 where each source/drain zone comprises a main source/drain portion and a more lightly doped source/drain extension laterally continuous with the main source/drain portion, the source/drain extensions of the two source/drain zones of each transistor terminating its channel zone along the semiconductor body's major surface.

31. A structure as in Claim 8 further including a normally off p-channel further insulated-gate field-effect transistor ("IGFET") comprising a pair of laterally separated p-type source/drain zones situated in the semiconductor body along its major surface, a channel zone extending between the p-channel further IGFET's source/drain zones in the semiconductor body along its major surface, a gate electrode situated over the channel zone of the p-channel further IGFET and extending partially over its source/drain zones, and a gate dielectric layer separating the gate electrode of the p-channel further IGFET from its source/drain and channel zones, the gate dielectric layers of the n-channel CJIGFET and the p-channel further IGFET both being thicker than the gate dielectric layers of the two SCIGFETs.

32. A structure as in Claim 31 wherein:

the gate dielectric layers of the two SCIGFETs are of approximately equal thickness; and

the gate dielectric layers of the n-channel CJIGFET and the p-channel further IGFET are of approximately equal thickness.

33. A structure as in Claim 31 wherein the n-channel CJIGFET and the p-channel further IGFET are each of greater channel length than each SCIGFET.

34. A structure as in Claim 31 wherein the channel zone of the p-channel further IGFET is n-type such that the p-channel further IGFET is an SCIGFET.

35. A structure as in Claim 34 wherein:

the gate electrode of the n-channel SCIGFET comprises n-type semiconductor material; and

the gate electrodes of the p-channel SCIGFET, the n-channel CJIGFET, and the p-channel further IGFET comprise p-type semiconductor material.

36. A structure as in Claim 31 wherein the channel zone of the p-channel further IGFET is p-type and is more lightly doped than its source/drain zones such that the p-channel further IGFET is a CJIGFET.

37. A structure as in Claim 36 wherein:

the gate electrodes of the n-channel SCIGFET and the p-channel further IGFET comprise n-type semiconductor material; and

the gate electrodes of the p-channel SCIGFET and the n-channel CJIGFET comprise p-type semiconductor material.

38. A structure as in Claim 31 wherein the n-channel CJIGFET conducts current through a field-induced channel.

39. A structure as in Claim 31 wherein the n-channel CJIGFET conducts current through metallurgical channel.

40. A structure as in Claim 31 wherein the channel zone of each SCIGFET is part of body material having a net dopant concentration which reaches a primary local subsurface maximum below a channel surface depletion region that extends along the semiconductor body's major

surface into that channel zone but no more than 0.4 μm below the semiconductor body's major surface.

41. A structure as in Claim 31 wherein the source/drain and channel zones of the n-channel CJIGFET form a composite pn junction with body material having a net dopant concentration which reaches a primary local subsurface maximum below the channel zone but no more than 0.6 μm below the semiconductor body's major surface.

42. A structure as in Claim 31 wherein the channel zone of each SCIGFET is part of body material having a net dopant concentration which reaches a primary local subsurface maximum below a channel surface depletion region that extends along the semiconductor body's major surface into that channel zone but no more than 0.4 μm below the semiconductor body's major surface.

43. A method comprising:

selectively introducing channel-zone-defining n-type semiconductor dopant into a semiconductor body to define an n-type region that includes a surface-adjoining n-type channel zone for a normally off n-channel channel-junction insulated-gate field-effect transistor ("CJIGFET");

providing the semiconductor body with (a) a gate dielectric layer for an n-channel surface-channel insulated-gate field-effect transistor ("SCIGFET") and (b) a gate dielectric layer for the n-channel CJIGFET along its channel zone;

providing (a) a gate electrode for the n-channel CJIGFET over its gate dielectric layer and (b) a gate electrode for the n-channel CJIGFET over its gate dielectric layer; and

selectively introducing (a) source/drain-defining n-type semiconductor dopant into p-type material of the semiconductor body to define, for the n-channel SCIGFET, a pair of laterally separated surface-adjoining n-type source/drain zones between which a surface-adjoining p-type channel zone extends along the gate dielectric layer for the n-channel SCIGFET such that its gate dielectric layer overlies its channel zone, partially overlies its source/drain zones, and is separated from its source/drain and channel zones by its gate dielectric layer and (b) source/drain-defining n-type semiconductor dopant into the semiconductor body to define, for the n-channel CJIGFET, a pair of laterally separated surface-adjoining n-type source/drain zones between which the n-type channel zone for the n-channel CJIGFET extends such that its gate electrode overlies its channel zone, partially overlies its source/drain zones, and is separated from

its source/drain and channel zones by its gate dielectric layer and such that the channel zone of the n-channel CJIGFET is more lightly doped than its source/drain zones.

44. A method as in Claim 43 wherein:

the gate electrode of the n-channel SCIGFET comprises n-type semiconductor material; and

the gate electrode of the n-channel CJIGFET comprises p-type semiconductor material.

45. A method as in Claim 44 wherein the gate electrode of the n-channel CJIGFET is made p-type prior to defining its source/drain zones.

46. A method as in Claim 43 wherein the gate dielectric layer of the n-channel CJIGFET is thicker than the gate dielectric layer of the n-channel SCIGFET.

47. A method as in Claim 43 wherein the channel-zone-defining and source/drain-defining n-type dopants comprise arsenic.

48. A method as in Claim 43 further including:

providing the semiconductor body with a gate dielectric layer for a p-channel SCIGFET;

providing a gate electrode for the p-channel SCIGFET over its dielectric layer; and

selectively introducing source/drain-defining p-type semiconductor dopant into n-type material of the semiconductor body to define, for the p-channel SCIGFET, a pair of laterally separated surface-adjoining p-type source/drain zones between which a surface-adjoining n-type channel zone extends along the gate dielectric layer for the p-channel SCIGFET such that its gate electrode overlies its channel zone, partially overlies its source/drain zones, and is separated from its source/drain zones by its gate dielectric layer.

49. A method as in Claim 48 wherein:

the gate electrodes of the n-channel SCIGFET comprises n-type semiconductor material; and

the gate electrode of the p-channel SCIGFET and the n-channel CJIGFET comprise p-type semiconductor material.

50. A method as in Claim 49 wherein the gate electrode of the n-channel CJIGFET is made p type prior to defining its source/drain zones.

51. A method as in Claim 48 wherein the channel-zone-defining and source/drain-defining n-type dopants comprise arsenic.

52. A method as in Claim 48 wherein the gate dielectric layer of the n-channel CJIGFET is thicker than the gate dielectric layers of the two SCIGFETs.

53. A method as in Claim 52 wherein the gate-dielectric-layer-providing acts comprise:

forming a first dielectric layer along the semiconductor body at least along the lateral locations for the three gate dielectric layers;

removing largely all the material of the first dielectric layer generally along the lateral locations for the gate dielectric layers of the two SCIGFETs; and

forming a second dielectric layer along the semiconductor body at least along the lateral locations for the gate dielectric layers of the two SCIGFETs such that (a) the gate dielectric layers of the two SCIGFETs respectively comprise a pair of laterally separated portions of the second dielectric layer and (b) the gate dielectric layer of the n-channel CJIGFET comprises a portion of remaining material of the first dielectric layer.

54. A method as in Claim 53 wherein the second dielectric layer is thinner than the first dielectric layer.

55. A method as in Claim 53 wherein the acts of forming the first and second dielectric layers comprise reacting oxygen with material of the semiconductor body such that each gate dielectric layer comprises semiconductor material and oxygen.

56. A method as in Claim 55 wherein the act of forming the first dielectric layer further includes reacting nitrogen with material of the semiconductor body such that the gate dielectric layers of the two SCIGFETs further include nitrogen.

57. A method as in Claim 53 further including before forming the first dielectric layer:

thermally oxidizing material of the semiconductor body along at least the lateral locations for the three gate dielectric layers to form a sacrificial dielectric layer; and

substantially removing the sacrificial dielectric layer.

58. A method as in Claim 57 further including, between forming the sacrificial dielectric layer and forming the first dielectric layer, removing a layer of material of the semiconductor body along at least the lateral location of the gate dielectric layer for each SCIGFET.

59. A method as in Claim 53 wherein the gate-electrode-providing acts comprise:

depositing, subsequent to forming the second dielectric layer, a semiconductor layer over the second dielectric layer and the remaining material of the first dielectric layer; and

patterning the semiconductor layer and doping it selectively with n-type and p-type semiconductor dopants to define the three gate electrodes such that (a) the gate electrode of the n-channel SCIGFET comprises n-type material of the semiconductor layer and (b) the gate electrodes of the p-channel SCIGFET and the n-channel CJIGFET comprise p-type material of the semiconductor layer.

60. A method as in Claim 52 wherein the gate-dielectric-layer-providing and gate-electrode-providing acts comprise:

forming a first dielectric layer along the semiconductor body at least along the lateral locations for the three gate dielectric layers;

depositing a first semiconductor layer over the first dielectric layer;

removing largely all the material of the first semiconductor layer and the first dielectric layer generally along the lateral locations for the gate dielectric layers of the two SCIGFETs;

forming a second dielectric layer along the semiconductor body at least along the lateral locations for the gate dielectric layers of the two SCIGFETs such that (a) the gate dielectric layers of the two SCIGFETs respectively comprise a pair of laterally separated portions of the second dielectric layer and (b) the gate dielectric layer of the n-channel CJIGFET comprises a portion of remaining material of the first dielectric layer;

depositing a second semiconductor layer over at least the second dielectric layer; and

patterning the two semiconductor layers and doping them selectively with n-type and p-type semiconductor dopants to define the three gate dielectric layers such that (a) the gate electrode of the n-channel SCIGFET comprises n-type material of the second semiconductor layer, (b) the gate electrode of the p-channel SCIGFET comprises p-type material of the second semiconductor layer, and (c) the gate electrode of the n-channel CJIGFET comprises p-type material of the first semiconductor layer.

61. A method as in Claim 60 wherein the first dielectric layer is thicker than the second dielectric layer.

62. A method as in Claim 60 wherein the acts of forming the first and second dielectric layers comprise reacting oxygen with material of the semiconductor body such that each gate dielectric layer comprises semiconductor material and oxygen.

63. A method as in Claim 62 wherein the act of forming the first dielectric layer further includes reacting nitrogen with material of the semiconductor body such that the gate dielectric layers of the two SCIGFETs further include nitrogen.

64. A method as in Claim 60 wherein:

the second dielectric-layer-forming act includes forming a barrier dielectric layer along the remaining material of the first dielectric layer along at least the lateral location for the gate dielectric layer of the n-channel CJIGFET; and

the patterning and doping act includes removing material of the second semiconductor layer overlying the remainder of the first semiconductor layer using the barrier dielectric layer to substantially prevent the remaining material of the first semiconductor layer from being removed.

65. A method as in Claim 60 further including before forming the first dielectric layer:

thermally oxidizing material of the semiconductor body along at least the lateral locations for the three gate dielectric layers to form a sacrificial dielectric layer; and

substantially removing the sacrificial dielectric layer.

66. A method as in Claim 65 further including between forming the sacrificial dielectric layer and forming the first dielectric layer, removing a layer of material of the semiconductor body along at least the lateral location of the gate dielectric layer for each SCIGFET.

67. A method as in Claim 48 wherein the channel zone of each SCIGFET has a location for a channel surface depletion region which extends into that channel zone during operation of that SCIGFET, the method further including prior to defining lateral shapes for the gate electrodes of the two SCIGFETs:

introducing primary p-type semiconductor dopant into the semiconductor body such that the primary p-type dopant reaches a maximum concentration below the location for the channel surface depletion region of the n-type SCIGFET but no more than 0.4 μm deep into the semiconductor body; and

selectively introducing primary n-type semiconductor dopant into the semiconductor body such that the primary n-type dopant reaches a maximum concentration below the location for the channel surface depletion region of the p-type SCIGFET but no more than 0.4 μm deep into the semiconductor body.

68. A method as in Claim 67 further including prior to defining the lateral shapes for the gate electrodes of the two SCIGFETs:

selectively introducing a pair of additional p-type semiconductor dopants into the semiconductor body such that the additional p-type dopants respectively reach maximum concentrations deeper at vertically separated locations deeper into the semiconductor body than where the primary p-type dopant reaches its maximum concentration; and

selectively introducing a pair of additional n-type semiconductor dopants into the semiconductor body such that the additional n-type dopants respectively reach maximum concentrations at vertically separated locations deeper into the semiconductor body than where the primary n-type dopant reaches its maximum concentration.

69. A method as in Claim 48 further including, prior to defining a lateral shape for the gate electrode of the n-channel CJIGFET, introducing primary p-type semiconductor dopant into the semiconductor body such that the primary p-type dopant reaches a maximum concentration below the channel zone of the n-channel CJIGFET but no more than 0.6 μm deep into the semiconductor body.

70. A method as in Claim 69 further including, prior to defining the lateral shape for the gate electrode of the n-channel CJIGFET, introducing a pair of additional p-type semiconductor dopants into the semiconductor body such that the additional p-type dopants respectively reach maximum concentrations at vertically separated locations deeper into the semiconductor body than where the primary p-type dopant reaches its maximum concentration.

71. A method as in Claim 48 wherein, subsequent to providing the gate electrodes for the two SCIGFETs, the semiconductor body has a major surface along which the channel zones for the two SCIGFETs extend, the method including further including subsequent to defining lateral shapes for the gate electrodes of the two SCIGFETs:

introducing further p-type semiconductor dopant into at least the location for the p-type channel zone of the n-channel SCIGFET such that the further p-type dopant reaches a local minimum surface concentration along the semiconductor body's major surface at a location between the n-channel SCIGFET's source/drain zones; and

introducing further n-type semiconductor dopant into at least the location for the n-type channel zone of the p-channel SCIGFET such that the further n-type dopant reaches a local minimum surface concentration along the semiconductor body's major surface at a location between the p-channel SCIGFET's source/drain zones.

72. A method as in Claim 71 wherein the act of introducing each further dopant comprises implanting ions of a species of that dopant at a tilt angle of at least 15° relative to a direction generally perpendicular to the semiconductor body's major surface.

73. A method as in Claim 48 further including:

providing the semiconductor body with a gate dielectric layer for a normally off p-channel further insulated-gate field-effect transistor ("IGFET");

providing a gate electrode for the p-channel further IGFET over its gate dielectric layer; and

selectively introducing source/drain-defining p-type semiconductor dopant into n-type material of the semiconductor body to form, for the p-channel further IGFET, a pair of laterally separated surface-adjoining source/drain zones between which a surface-adjoining channel zone extends along the gate dielectric layer for the p-channel further IGFET such that its gate electrode overlies its channel zone, partially overlies its source/drain zones, and is separated from its source/drain and channel zones by its gate dielectric layer.

74. A method as in Claim 73 wherein the acts of providing the gate electrodes comprise:

substantially simultaneously depositing material for the gate electrodes of the n-channel CJIGFET and the p-channel further IGFET; and

substantially simultaneously depositing material for the gate electrodes of the two SCIGFETs such that the gate electrodes of the n-channel CJIGFET and the p-channel further IGFET are thicker than the gate electrodes of the two SCIGFETs.

75. A method as in Claim 73 wherein the n-channel CJIGFET and the p-channel further IGFET are each formed at greater channel length than each SCIGFET.

76. A method as in Claim 73 wherein the channel zone of the p-channel further IGFET is n-type such that the p-channel further IGFET is formed as a surface-channel IGFET.

77. A method as in Claim 76 wherein:

the gate electrode of the n-channel SCIGFET comprises n-type semiconductor material; and

the gate electrodes of the p-channel SCIGFET, the n-channel CJIGFET, and the p-channel further IGFET comprise p-type semiconductor material.

78. A method as in Claim 73 further including selectively introducing channel-zone defining p-type semiconductor dopant into the semiconductor body to define a p-type region that includes a p-type channel zone for the p-channel further IGFET such that (a) the channel zone of the p-channel further IGFET is more lightly doped than its source/drain zones and (b) the p-channel IGFET is formed as a channel-junction IGFET.

79. A method as in Claim 78 wherein:

the gate electrodes of the n-channel SCIGFET and the p-channel further IGFET comprise n-type semiconductor material; and

the gate electrodes of the p-channel SCIGFET and the n-channel CJIGFET comprise p-type semiconductor material.

80. A method as in Claim 78 wherein the gate electrodes of the n-channel CJIGFET and the p-channel further IGFET are respectively made p-type and n-type prior to forming their source/drain zones.